

SEMICONDUCTOR PACKAGE STRUCTURE REDUCING WARPAGE AND
MANUFACTURING METHOD THEREOF

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Abstract of the Disclosure

An electrical substrate useful for semiconductor packages is disclosed. The electrical substrate includes a core insulative layer. A first surface of the insulative layer has circuit patterns thereon. Some of the circuit patterns are stepped in their heights from the first surface, in that a first subportion of the circuit pattern, including a ball land, extends further from the first surface than a second subportion of the same circuit pattern, and also extends further from the first surface than a ball land of other circuit patterns. Accordingly, solder balls fused to the ball lands of the stepped circuit patterns extend further from the first surface than same-size solder balls fused to the ball lands of the non-stepped circuit patterns, thereby circumventing electrical connectivity problems that may arise from warpage of the electrical substrate.